HT26 - 11001A

mycom

DMP1040

Super High Speed Pulse Generator LSI

100 pin QFP

[Outline of Specifications]

mycom, Inc

Introduction

This Outline of Specifications summerizes various functions of the Pulse Generator LSI, MPG1040.

Its specifications may change. Please contact our Business Offices for details.

-960412-

Contents

1. Outline of Functions

1-1. Name of Product

MPG1040

1-2. Shape

100 pin QFP

1-3. Outline of Functions

MPG1040 is a version up-ed LSI based on the pulse generator LSI, MPG1030, made by our firm.

Newly added and strengthened functions are described below.

<Any Pattern Acceleration/deceleration>

1. Any pattern acceleration/deceleration is protected and guaranteed when
   a. deceleration command goes into effect during acceleration and when
   b. triangle drive is active.

2. It is possible to perform any pattern acceleration / deceleration using the built-in memory data.
   a. Resolution: 32, 64
   b. Perfectly any pattern can be set.
   c. Any slope acceleration / deceleration by using self-starting, maximum frequency, average slope setting and slope data is possible.

<Buffering>

3. Buffering Function
   a. Selection Mode: Drive parameter sets can be selected using commands.
   b. Sequence Mode: Parameter sets set are executed sequentially. Repeated drive, continuous linear interpolation, and Home Search are conducted.

<Override>

4. Speed Override Function
   It is possible to rewrite the maximum speed in action of a register (target speed).

< Pass >

5. I/O used for pass action and its processing function is available.

< I/O >

6. Data bus of 32, 16, and 8 bits is used.

7. I/O Terminals
   a. Logic switching
   b. Switching between edge trigger and level latch
   c. Masking of terminals

8. There are 8 each of general purpose I/O's.

9. Interrupt outputs are made into one (INT). Daisy-chained.

10. Clock Mode (1/2 clock) is handled by software commands.

11. Stepping /servo motor selection is handled by software commands.

12. Slowdown input terminals for Reverse / Forward directions (RDWN,FDWN)

13. Slowdown stop input terminal for Reverse / Forward directions (RSST. FSST)

<Home Search>

14. Home Search
    a. 2 systems of Z and ORG are used for the Home Search function. They are selected by commands.
    b. The count of 0~255 is used for Z/ORG. An interrupt is outputted when a set number is reached.

<Encoder Counter>

15. 32-bit encoder counter is used.
    a. Multiplying is set by software commands.
    b. Inputs are switched between external (Encoder output) and internal (Self output pulse)
    c. Multiple's function for the counter values

<General Purpose Counter>

16. General purpose counters: 8bit x 7
    a. Each has 8bit compare circuit.
    b. Maximum 56bit counter using any combination is possible.
    c. Dwell timer (32bit) capable of time setting
    d. Deviation Counter (24bit)
    e. The operational clock is selectable between external and internal (Standard clock 1/1 ~ 1/4096)

17. Deviation Counter · Clear output terminal. Self-generated.

18. Deviation Decision function. The number of output pulses and the value of the Encoder Counter are compared.

< Others >

19. The output pulses are divided. 1 ~ 256

20. The number of output pulses is set to 0~16, 777, 215, or infinity.

21. When the operation ends abnormally, the remaining pulses are used to restart.

22. Temporary Stop function (Pose) while pulses are outputted is available.

23. Outputting pulses starts at the same time the activation starts.

24. Deceleration Starting Point
    a. Automatic and manual operations are used.
    b. Masking of the Deceleration Starting Point Register (D) is used.
    c. The D Register is used to issue the deceleration start command when the Output Pulse Infinite Mode is used.

25. Multiple Axes Sync Start

2. I/O Terminals

2-1. Input Terminals

Terminals	Names	
1	CLK	Standard Clock input terminal
2	/RST	RESET terminal
3	/CS	Chip Select input
4	/WR	Write Enable terminal
5	/RD	Read Enable terminal
6	MR	Memory/Register Select terminal
7 ~ 14	A (7:0)	Address Bus
15	ALM	Alarm input Maskable Logic is switchable Level latch
16	REV	Reverse overrun input, maskable, Logic is switchable Level latch
17	FOR	Forward overrun input, maskable, Logic is switchable Level latch
18	ES	Emergency Stop, maskable, Logic is switchable
19	RDWN	Reverse direction slowdown input, maskable, Logic is switchable, Edge trigger / level latch switchable. The edge trigger is switchable between positive and negative.
20	FDWN	Forward direction slowdown input, maskable, Logic is switchable, Edge trigger / level latch switchable. The edge trigger is switchable between positive and negative.

21	RSST	Reverse direction slowdown stop input Maskable, logic is switchable, level latch
22	FSST	Forward direction slowdown stop input Maskable, logic is switchable, level latch
23	NEAR	NEAR input, maskable, logic is switchable, edge trigger (positive/negative switchable)
24	Z	Z-phase input. Z or ORG is selected by commands. Maskable. Logic is switchable. Edge trigger and level latch are switchable. Edge trigger is switchable between positive and negative.
25	ORG	ORG input. Z or ORG is selected by commands. Maskable. Logic is switchable. Edge trigger and level latch are switchable. Edge trigger is switchable between positive and negative.
26	INP	In position input. Maskable. Logic is switchable. Edge trigger and level latch are switchable. Edge trigger is switchable between positive and negative
27	PAUS	Temporary stop. Multiple axes sync start. Maskable. Logic is switchable. Level latch.
28	EA	Encoder Phase A input. Maskable. Logic is switchable.
29	EB	Encoder Phase B input. Maskable. Logic is switchable.
30	CINT	Daisy chain interrupt signal input. This terminal is used to daisy-chain multiple axes interrupt request signal.
31 ~ 38	IP (7:0)	General purpose inputs. Maskable. Logic is switchable. Interrupt request is outputted by setting up commands.

2-2. Bi-directional Terminals

Number of terminals	Terminal names	
39	IOCP	Linear interpolation pulse I/O
40 ~ 71	D (31:00)	Data bus

2-3. Output Terminals

Number of terminals	Terminal names	
72	INT	Interrupt output. Maskable. Logic is switchable. This output includes the following: * Each error input stop * Each encoder counter interrupt * General purpose counter compare interrupt * Data request * Encoder counter over/under flow interrupt These elements are maskable individually.
73	PINT	Pseudo end signal used for bus
74	MOVE	Operation Monitor. Maskable. Logic is switchable.
75	PCW	CW pulse output terminal. Maskable. Logic is switchable.
76	DCCW	CCW pulse output terminal or direction output. Maskable. Logic is switchable.
77	HCLR	Deviation Counter Clear signal. Maskable. Logic is switchable.
78	RC	Output pulse count · outputted when all is Fh. Maskable. Logic is switchable.
79 ~ 86	OP (7:0)	General purpose outputs.

3. Description of Functions

3-1. Protection and Guarantee of Any Acceleration / Deceleration Patterns

3-1-1 Deceleration during Acceleration

If a deceleration command is issued while the machine is accelerating under Any pattern (S-letter), and if the operation moves to the even speed or deceleration, there will be a stress greater than at the time of trapezoid drive is placed on the driving system.

In order to avoid the above, MPG1040 starts deceleration after moving into the even speed state by giving it a curve. The deceleration pattern between the speeds V2 and S at this time is guaranteed. [Fig. 1 and 2]

It is also possible to select by a command to start deceleration at the time when the command is issued. However, the pattern of acceleration is not protected at this time. [Fig. 3]

Fig. 1 Fig. 2 Fig. 3 Fig. 4

Deceleration
command issued

Deceleration
command issued

Deceleration
command issued

3-1-2 Guarantee of Pattern during Triangle Drive

The deceleration starts when the number of output pulses reach about 1/2 of the set number during the automatic deceleration starting point mode. The pulse generator designed by our firm according to the specifications giving the highest preference to the number of pulses will start deceleration even if it is in the middle of acceleration. Naturally, the acceleration pattern is not guaranteed.

Thus, MPG1040 will correct the highest frequency to an appropriate value using the automatic calculation in order to perform acceleration / deceleration using the pattern suitable for the number of pulses and will start operation.

The average values of P3 and P2 are the same

Fig. 1

Max. frequency calculated auto-matically

Pattern of pulse number P1

Pattern of pulse number P2

Pattern of pulse number P3

The pulse No. P3 is not enough to reach the highest speed set (target speed). Therefore, the V is calculated automatically to a proper value and used.

The shape of the dotted line above is the shape obtained when a proper maximum speed (target speed) was not generated automatically.

3-2. Any Pattern Acceleration / Deceleration by Built-in Memory Data

3-2-1 Resolution

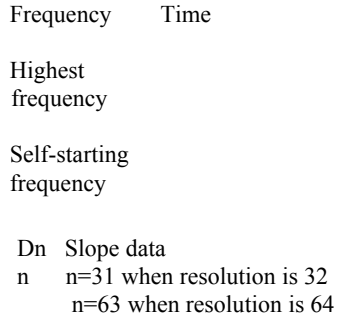
The Any Acceleration / Deceleration resolution between the self-activation and the highest frequency is 32 and 64.

3-2-2 Perfect Any Setup

Any data can be set in the entire interval for the acceleration/ deceleration pattern.

The data switching timing is generated within the LSI automatically. The driving time per 1 data is the same.

Fig. 5 Perfect any pattern setting acceleration / deceleration image (when accelerating)



3-2-3 Method of Driving

Any pattern acceleration / deceleration drive uses the following parameters.

a. Self-activating frequency
b. Highest frequency
c. The average acceleration (deceleration) slope value (It is OK when accelerating ≠ decelerating)
d. Slope data

The average acceleration (deceleration) slope value and the slope data are interrelated.

When driving with the slope data set from one of the functions, the average acceleration (deceleration) slope value is obtained from that function.

When multiple functions are used to set the slope data (as above),

the average acceleration (deceleration) slope = (Sum of all slope data) / Resolution number

3-3. Buffering Function

There are 3 buffers available.

			Buffer 0	Buffer 1	Buffer 2
1	Self-activating frequency	2 bytes	S_0	S_1	S_2
2	Maximum frequency	2 bytes	V_0	V_1	V_2
3	Acceleration slope	2 bytes	$G1_0$	$G1_1$	$G1_2$
4	Deceleration slope	2 bytes	$G2_0$	$G2_1$	$G2_2$
5	Amount of movement	3 bytes	P_0	P_1	P_2
6	Deceleration starting point	3 bytes	D_0	D_1	D_2
7	Amount of Interpolation movement	3 bytes	A_0	A_1	A_2
8	Command A	1 bytes	$CMDA_0$	$CMDA_1$	$CMDA_2$
9	Command B	1 bytes	$CMDB_0$	$CMDB_1$	$CMDB_2$

There are Select Mode and Sequence Mode as shown below.

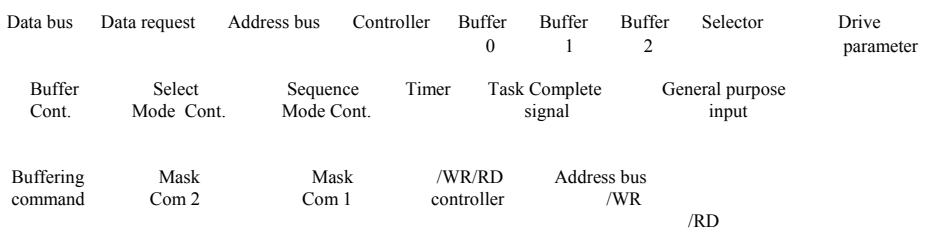


Fig. 6

3-3-1 Selection Mode

The drive starts when RUN=1 is written into the command of the buffer set you want to activate after writing the parameter set into the buffer before activating. It is also possible to activate using the specified set from the general purpose input.

Each parameter can be masked. Besides those which can be forced to be masked by the drive mode (deceleration starting point automatic calculation and interpolation), there are those that can be masked at will. The register that was masked will have data written into its buffer 0.

When 1 task ends, the end interrupt is outputted to outside.

3-3-2 Sequence Mode

Normally, the activation is followed by accessing the buffer sets in the order of 0->1->2->0 and the drive continues. The Task Complete signal causes the buffer access to switch. It is possible to have intervals between tasks.

Each parameter register can be masked. The masked register will have the value of the previous buffer in it (0 ->1, 1 ->2, 2 ->0).

If the data is empty or RUN=0 is detected, the sequential operation comes to an end and an End Interrupt is issued.

3-4. Override Function

3-4-1 Conditions

a. Override is limited to the highest frequency (target speed) setting register, V, only.
b. The value to be overridden must always be larger than the value set for the self-activating frequency.

3-4-2 Basic Operation

c. The up/down of the output frequency is conducted by the override of the maximum frequency. The override is not accepted after the deceleration start command has been issued. The deceleration start command is generated by a command, an input terminal, deceleration starting point self-operation, and the deceleration starting point register. Namely, the override becomes invalid when deceleration starts towards the self-starting frequency already set.

d. It is possible to write the override timing at any time, however, the action caused by the above takes place after the constant speed of the targeted frequency prior to the override is reached (Fig. 7 and 8).

Fig. 7

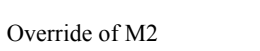


Fig. 8

3-4-3. Override is valid when the deceleration starting point automatic calculation mode is used

also. The deceleration starting point is calculated automatically from the number of pulses used for each acceleration/deceleration interval.

3-5. Bus Operation

The main operation of the Bus Operation is performed by the software of the Host (CPU). MPG1040 is capable of interfacing with the Host and sending commands to the axes (secondary axes bus).

This is called the "pseudo main axis bus".

If 2 axes are used with the actual bus operation, there will be 3 MPG1040's needed. Two of them will be generating drive pulses (Bus for secondary axes) and one will be the "pseudo main axis bus".

The Bus Operation involves writing the amount of movement into the "pseudo main axis bus" and "Bus for secondary axes". The Bus Operation continues as long as there is writing of the moving amount.

The deceleration starting point is written into the Deceleration Starting Point Register of the

"pseudo main axis bus". The Deceleration Starting Point Register is updated when the moving amount is written in. When the pay out pulses of the "pseudo main axis bus" reaches the deceleration starting point, all axes run by the bus start decelerating.

3-6. Home Search

3-6-1 Exclusive Terminal

NEAR· Z· ORG was created as the input terminal used for Home Search.

Z/ORG is selected by a command.

3-6-2 Complete Signal

The Z/ORG input is counted up to 255.

When the value counted reaches the value set in the Compare Register (8bit), the Home Search Complete signal is outputted.

3-6-3 Deviation Counter · Clear Output

This is outputted when the Home Search is completed.

3-6-4 Dwell Timer

This is used to monitor the imposition signal from the servo driver, etc. using the general purpose counter built in MPG1040. This is to avoid the run away of software.

3-7. Deceleration Starting Point

MPG1040 has automatic and manual modes for deceleration starting point calculation.
The Deceleration Starting Point Register (D) is masked when the manual mode is used.
The D Register can be used to start deceleration when the infinite pulse output is used also.

3-8. Setting Up the Number of Output Pulses

3-8-1 Setting Up

The number of output pulses can be set as 0 ~ 16, 777, 215, or infinite.
It is possible to set 0. If this is done, there will be no pulse outputted even if the machine is activated. The use of continuous linear interpolation drive and the bus drive have been taken into consideration.

3-8-2 Processing the Remaining Pulses

When the machine is stopped without finishing paying out due to the slowdown, errors, etc., it is possible to use the After Stop Command to perform operation using the remaining pulses.

3-9. Encoder Counter

3-9-1 Setting Up

The multiplication set up uses the software commands now.
EA and EB, the input terminals, receive outputs from the Encoder. However, it is possible now to take in pulse outputs, PCW · DCCW of its own using commands.

3-9-2 Interrupt Output

There are 4 interrupt outputs including the value set by the compare register. There is no limit on how many times the interrupt outputs can be used by rewriting the values of the compare register.

3-9-3 Counting Multiples

It is possible, using commands, to have x8, x4, x2, x1, x1/2, x1/4, x1/8, x1/16 multiples

count for the Input 1.

3-10. General Purpose Counter

3-10-1 Configuration

There are 7 8bit counters. Each one has its own compare circuits.
They can be joined together for any length using 8bit as the unit. Up to 56bit counter with the compare circuit can be used.

3-10-2 Operational Clock

It is possible to switch between external or internal clock to run the counter. If an internal clock is used, it is possible to use clocks divided from 1/1 ~1/4096.

3-10-3 Dwell Timer

The 32bit long general purpose counter specified is used. The values of this counter and the compare register are used to put the interrupt output into effect.

3-10-4 Deviation Counter

The 24bit long general purpose counter specified is used. The values of this counter and the compare register are used to put the interrupt output into effect.

3-10-5 Judgment on Deviation

Every time a task is completed, it is compared with the value of the Encoder Counter and the deviation is outputted.
The deviation can be either added or each task is cleared to 0.

3-11. Temporary Stop

During the time when pulses are outputted, it is possible to stop temporarily (pause) using any timing. We have taken into consideration the use of continuous linear interpolation drive and the bus drive.